A Quasi-Planar FET Amplifier in Integrated Finline and Microstrip Technique

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Abstract —**The design and performance of a single-stage 20 GHz GaAs FET amplifier in quasi-planar technology are described. The component includes a compact, wide-band transition between the finline input and output ports and the microstrip impedance-matching networks for the transistor. By virtue of a novel bias network which includes a microstrip bandstop filter and a 50 Ω resistor, this transition provides unconditional stability even at frequencies below cutoff of the finline ports. The overall amplifier has a gain of 6 dB at 20 GHz, and a 3 dB bandwidth of 17 percent.**

I. Introduction

Field effect transistors (FET's) and, more recently, high electron mobility transistors (HEMT's) are being used in the design of low-noise amplifiers in the 26.5 to 40 GHz frequency range [1]–[3]. In addition, a FET receiver at 30 GHz [4] and a 60 GHz FET amplifier [5] have been reported. This signals the movement of three-terminal active devices into the millimeter-wave frequency range, a region of the frequency spectrum previously dominated by two-terminal devices.

In this paper the design of a quasi-planar 20 GHz FET amplifier using a combination of finline and microstrip is described. However, the amplifier could be scaled to millimeter-wave frequencies without losing the advantages inherent in its design.

The layout of the complete amplifier is shown in Fig. 1. The transistor with its microstrip matching networks can be seen in the center. The finline input and output ports (in WR-42 enclosures) are coupled to the microstrip circuit via cross-shaped transitions. Each transition is terminated in a microstrip bandstop filter which serves as a bias network and guarantees unconditional stability even below the cutoff frequency of the finline ports.

Scattering parameters for the field effect transistor (NEC NE67300) were available from the manufacturer up to 18 GHz. Since it was desirable to predict its performance at higher frequencies, a device model was developed. Using this model, an unconditionally stable amplifier with a 3 dB bandwidth of 17 percent and about 6 dB of gain at 20 GHz was designed. In the following, the amplifier design will be described, and the measured performance of the amplifier will be presented.

II. Design of the Amplifier

In the design of this amplifier, a standard device model resident in the SUPER-COMPACT library [6] was used to characterize the NEC NE67300 and to predict its parameters up to 30 GHz.

Using the optimization capabilities of SUPER-COMPACT, the component values were determined in such a way that the computed S parameters of the model matched the manufacturer-supplied S parameters in the 2–18 GHz range.

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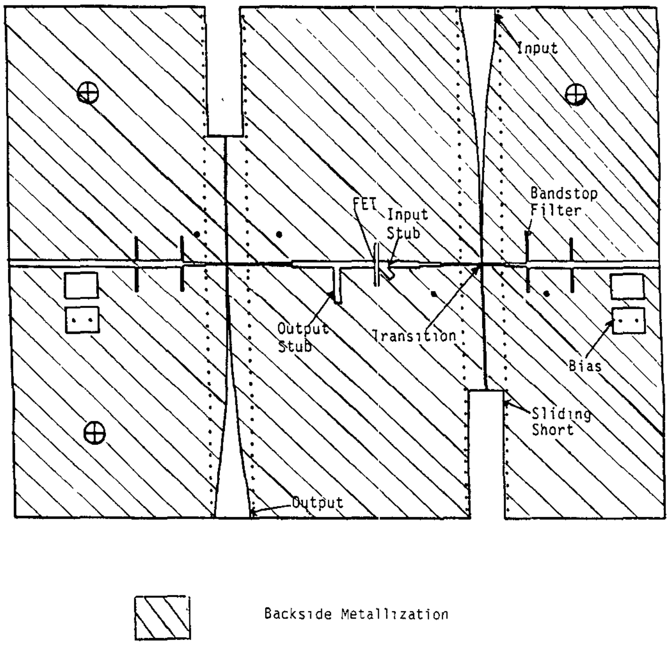

Fig. 1. Layout of the complete amplifier including transitions and biasing networks.

The amplifier itself was designed as a narrow-band high-gain device. The principal design goal was to achieve unconditionally stable operation. If desired, either the bandwidth or the noise figure of the amplifier could be improved. Since the finline-to-microstrip transition covers almost half a waveguide band, a wide-band matching network could be designed to increase the operating bandwidth of the amplifier.

A. Stability Analysis

Since the impedances of the finline ports become purely reactive below cutoff ($f_c = 7.41$ GHz), care must be taken to ensure that the transistor sees a stable load even in that frequency range. Fig. 2 shows the input and output stability circles of the transistor obtained with TOUCHSTONE [7]. The lower the frequency, the larger the area of instability becomes, and the input and output networks must be designed so as to avoid these regions at all frequencies. This will be described next.

B. Matching Network Design

The maximum available gain (MAG) of the transistor was found to be 6.8 dB at 20 GHz. The corresponding load and source terminations are, respectively,

$$\Gamma_{MS} = 0.79\angle -145^\circ \qquad \Gamma_{ML} = 0.46\angle 132^\circ .$$

These correspond to the following impedances and admittances (reference 50 Ω):

$$Z_{in} = (6.8 - j15.3)\,\Omega \qquad Z_{out} = (21.5 + j18.6)\,\Omega.$$

Single shunt-stub tuners were used to realize the input and output matching networks (see Fig. 1). The circuit was optimized with TOUCHSTONE over the range 19.5–20.5 GHz to yield optimum gain. The parameters which were allowed to vary were the input and output stub length and their distance to the FET. A minimum distance of 15 mils from the FET was enforced for feasibility. The stub lengths and positions were as follows: the input matching stub was 64 mils long and 15 mils from the bond

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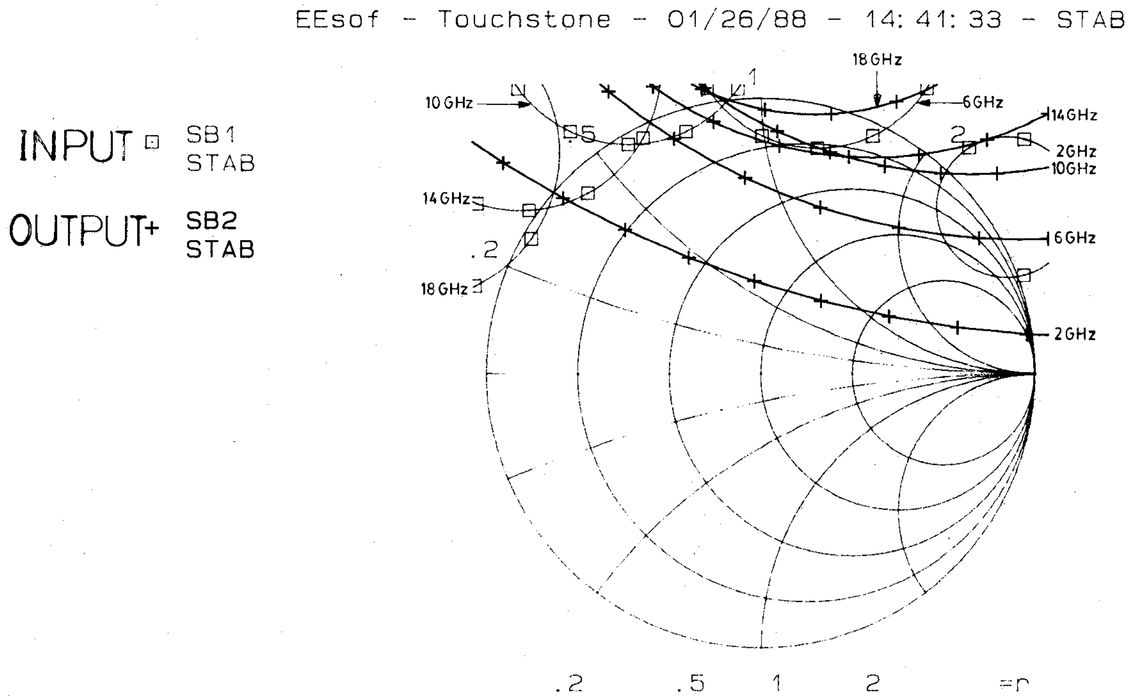


Fig. 2. Stability circles of the NEC NE67300 FET.

wires; the output stub was 197 mils from the bond wires and 164 mils long. Also, both matching networks included a quarter-wave transformer matching the 50 Ω amplifier terminals to the 121 Ω microstrip used in the microstrip-to-finline transitions, which will be described next.

C. The Finline-to-Microstrip Transition

With the finline-to-microstrip transition the amplifier can be integrated into a finline environment or, via an exponential taper, connected to waveguide.

Fig. 3 shows (a) the transition and (b) its equivalent circuit developed for this amplifier. It consists of a finline and microstrip crossing each other. At $\lambda/4$ from the junction, the finline is terminated in a short circuit, and the microstrip line in an open circuit. This transition is very similar to the microstrip-slot transition described by Chambers *et al.* [8] and discussed by Knorr [9]. Indeed, for very narrow gap finlines, the formulas for the equivalent circuit parameters found in [9] may be used without modification. Z_{0f} and Z_{0m} are the characteristic impedances of the finline and the microstrip. The value of the turns ratio n for the transformer is dependent on the fields in the finline, and is readily determined using the equations given by Knorr [9, eqs. (3)–(7)].

A finline of relatively low impedance (130 Ω) was chosen for the transition. It was low enough to match the microstrip assuming a small transformer ratio but not so low that the finline gap became too narrow to realize. Also, if the gap becomes too narrow, losses in the finline increase significantly. For a 130 Ω finline on 0.01-in-thick RT/Duroid ($\epsilon_r = 2.2$) in a WR-42 waveguide housing at 20 GHz, the slot width was found to be 0.15 mm. This configuration yields an ϵ_{eff} of 1.16. These data were generated using a transverse resonance program [10] which is appropriate for analyzing finlines with extremely narrow slots taking the effect of finite metallization thickness into account. Due to the extremely narrow finline gap, the foreshortening effect at the finline short circuit is negligible. The required open circuit terminating the microstrip at $\lambda/4$ from the transition is realized by the input impedance of the 20 GHz bandstop filter. It consists of a 78 Ω quarter-wave transformer, followed by two pairs of open 100 Ω quarter-wavelength stubs which are separated by a $\lambda/2$ long 50 Ω line (see Fig. 3). A 50 Ω resistor and a 36 pF capacitor terminate the filter section at the bias pad. The filter has low insertion loss below the cutoff frequency of the finline so that at low frequencies, the FET sees the 50 Ω terminating resistor, which represents a stable load at these frequencies.

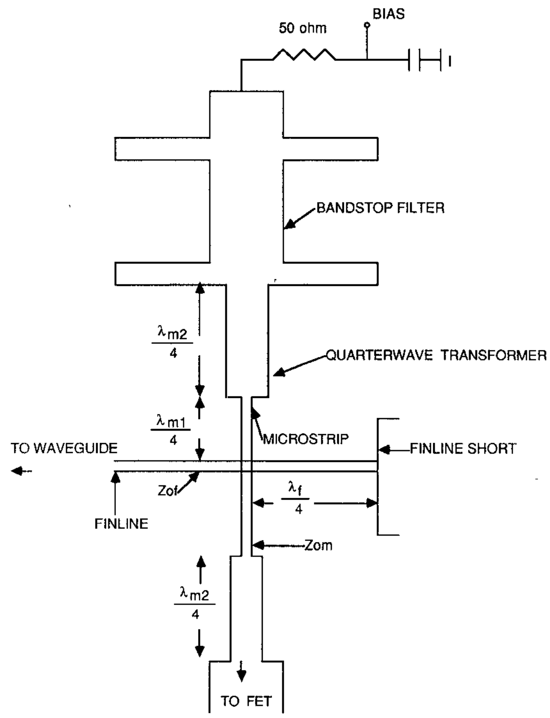
The fins were protected with a 6-μm-thick Mylar sheet. The optimum position for the short circuit is a quarter wavelength (2.8 mm) from the crossover point of the junction.

The complete transition was analyzed with TOUCHSTONE.

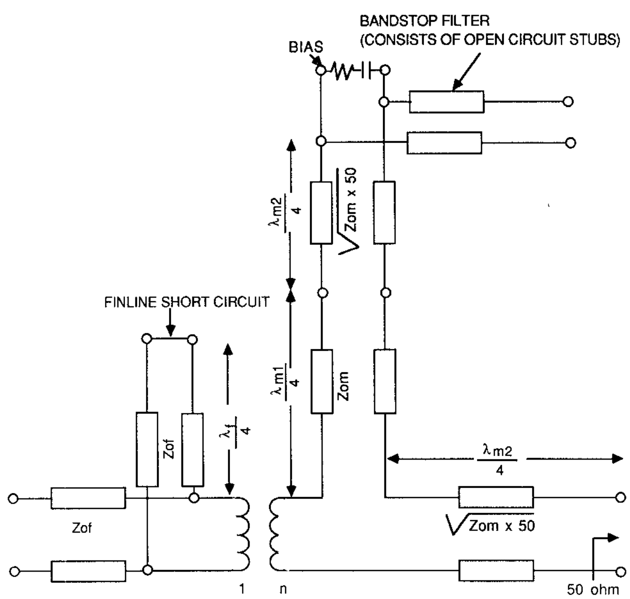
From the theoretical results a relatively broad-band transition was anticipated: less than 2 dB insertion loss over more than half the waveguide band. The predicted return loss was better than 25 dB at 20 GHz. To test the transition separately from the amplifier, a back-to-back-transition was fabricated and tested in the amplifier housing. The two transitions were separated by about half an inch of 50 Ω line. Fig. 4 shows the measured results obtained in this way, together with the theoretical response. The latter was obtained by neglecting conductor losses in the circuit. However, by assuming an average loss factor of 0.1 dB/wavelength in the transmission line, tapers, and filters, the difference of 1.5 dB between theory and measurement can be accounted for.

III. Amplifier Fabrication Technology

The circuit was fabricated using a thin-film process in which the copper cladding of the substrate (RT/Duroid 5880) is first removed by etching. Then the material is thermally stabilized, and a thin film of copper is sputtered onto the bare substrate. The circuit is imaged upon that layer using standard procedures and then etched. The etched circuit is plated to the desired metal thickness and then gold-flashed. Since a very thin layer of copper is being etched, fine lines and spaces as small as 0.001 in. can be realized with this technique. This process is also well suited for



(a)



(b)

Fig. 3. (a) Geometry and (b) equivalent circuit of the finline-to-microstrip transition.

the realization of the plated-through holes that can be seen along the finline sections in Fig. 1.

The amplifier was mounted in a split-block brass housing with milled WR-42 waveguide channels for the finline ports and sliding shorts (Fig. 5). The compartments housing the amplifier and the bias networks were accessible through removable covers for tuning and adjustment purposes.

The amplifier can be reduced considerably in size and weight by replacing the sliding shorts with printed short circuits, and by manufacturing the housing in metallized plastic, a technique which has been applied successfully in the realization of E plane power dividers [11]. The 50 Ω chip resistor in the bias network

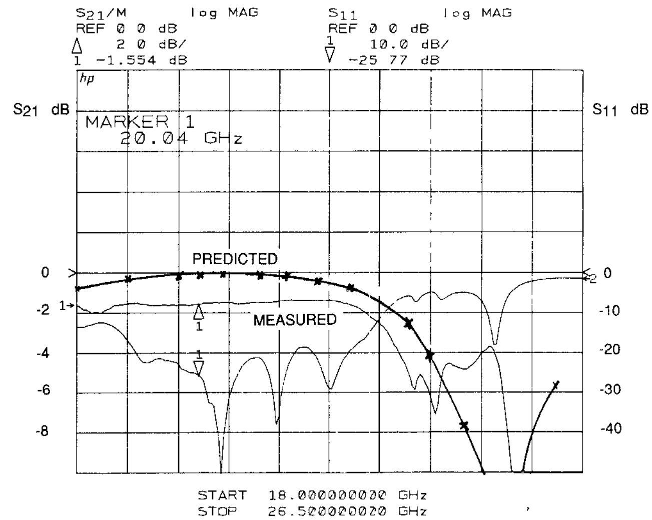
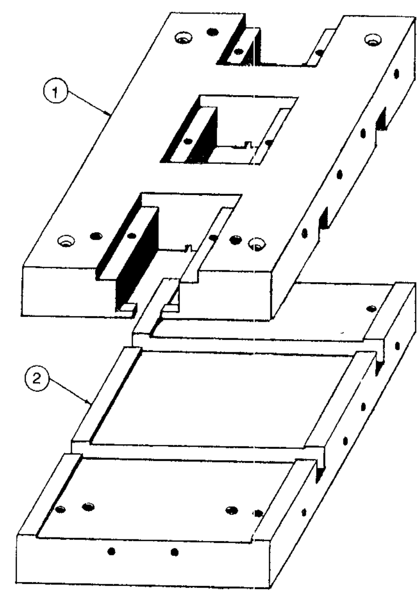
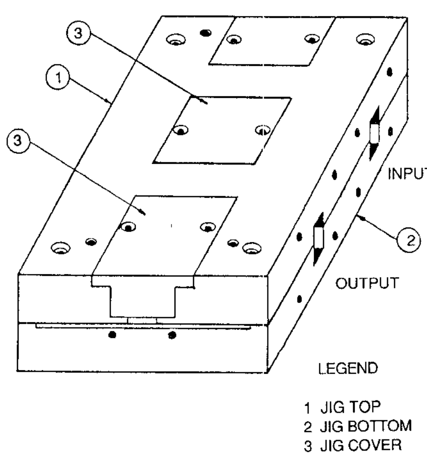


Fig. 4. Predicted and measured results for two back-to-back finline-to-microstrip transitions.



(a)



(b)

Fig 5. Split-block amplifier housing. (a) Disassembled. (b) Assembled

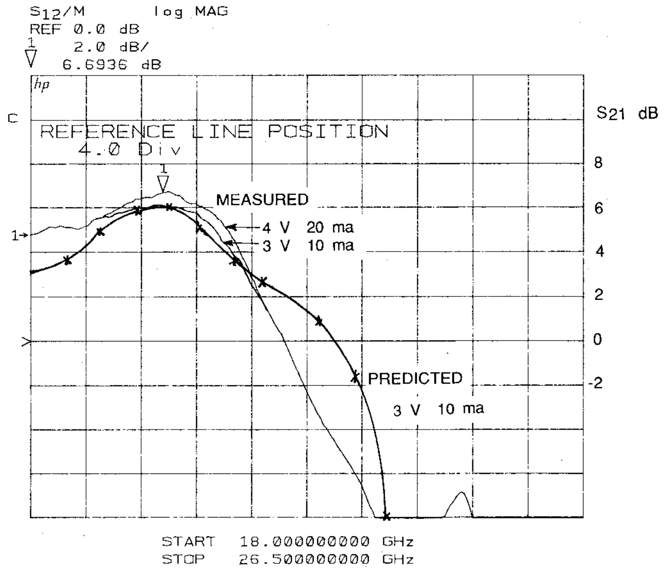


Fig. 6. Predicted and measured gain of the complete amplifier.

could also be replaced by depositing thin-film resistors directly onto the substrate. Furthermore, the circuit layout could easily be modified to realize an in-line version in which the RF input and output ports are aligned.

IV. Performance of the Complete Amplifier

Fig. 6 compares the measured response of the complete amplifier, including the finline tapers, with the response predicted with TOUCHSTONE. While the theoretical response was computed using S parameters for $V_{ds} = 3$ V and $I_{ds} = 10$ mA, measurements were performed for two bias points ($V_{ds} = 3$ V, $I_{ds} = 10$ mA, and $V_{ds} = 4$ V, $I_{ds} = 20$ mA), the latter measurement showing a maximum gain of 6.7 dB at 20 GHz. The 3 dB bandwidth was 3.4 GHz, or 17 percent.

Both input and output return losses were better than 10 dB at the center frequency. The isolation between input and output was better than 17 dB throughout.

V. Conclusion

The design of a single-stage 20 GHz GaAs FET amplifier in quasi-planar technology has been described. It features a novel combination of finline and microstrip. In particular, a compact, wide-band transition between the finline ports and the microstrip impedance matching networks has been developed and optimized. By virtue of the bias network including a microstrip bandstop filter and a 50 Ω resistor, this transition guarantees unconditional stability even at frequencies below cutoff of the finline ports.

Good agreement between the measured and calculated results demonstrates the validity of the design process as well as the quality of the fabrication technology. The amplifier can easily be integrated into a finline or a wave-guide environment. Alternatively, the transitions may be used in the realization of other components, such as oscillators and filters, requiring finline or waveguide ports.

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Dielectric Resonators Suitable for Use in Planar Integrated Circuits at Short Millimeter Wavelengths

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***Abstract* —This paper presents new experimental results of planar whispering gallery mode dielectric resonators. The three-dimensional field patterns obtained by using finite element techniques a well as measured resonant frequencies and quality factors carried out in the *Ka* (26.5–40 GHz) and 90–100 GHz bands are presented. The application to millimeter-wave components is also dealt with.**

I. Introduction

As millimeter-wave military and communications equipment demands dictate more compact packages and MIC compatibility, there is increasing interest in using dielectric resonator techniques in millimeter-wave oscillators and filters. However, at frequencies over 80 GHz, the dimensions of fundamental-mode cylindrical dielectric resonators which use the present-day low-loss and temperature stable dielectric materials become quite small and are very difficult to control. For these reasons, it is necessary to study new resonators making use of modes other than the fundamental.

In an early work [1], it was shown that whispering gallery (WG) mode dielectric resonators may be useful for millimeter-wave integrated circuits. It has also been found that planar dielectric resonators can be developed in a thin dielectric disk structure. This may be of interest from the standpoint of integrated circuit utilization. The present work is concerned with planar WG mode dielectric resonators excited by using mi-

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